ABSTRACT OF THE DISCLOSURE

A simulation system simulates an operation of a memory. This system includes an error generating step in addition to a memory operation simulating step. An error can easily be generated in a read/write operation of a memory model only by setting a memory address. A set of free bits, which is not used for the simulation of a memory operation, is used as a memory address for indicating the error generation. It is thus unnecessary to prepare a new description of a signal line exclusively for indication of error generation and it is possible to simulate a memory operation containing an error only by the normal descriptions of an address, data, and the like.